What is claimed is:

1. A system comprising:

a plurality of memory bus masters, each to generate an independent clock signal on respective outputs, each of said outputs connected by a transmission line to a common node, said common node additionally connected to a plurality of clock inputs of a memory array; and

an isolation circuit coupled between each of said transmission lines and said common node.

2. The system of claim 1, further comprising control inputs connected to said isolation circuit, to select one of said plurality of memory bus masters to drive a corresponding clock signal to said memory array while isolating the transmission lines of the other bus masters from said common node.

3. The system of claim 2, wherein said control inputs are supplied by a memory bus arbiter.

4. The system of claim 1, wherein said isolation circuit places a high impedance between said common node and said transmission lines.

5. The system of claim 1, wherein said isolation circuit comprises a plurality of FETs.

6. The system of claim 1, wherein said isolation circuit is a multiplexer.

7. In a computer board layout including a memory array and plurality of memory bus masters, a method comprising:

connecting each of said bus masters to a common node via a transmission line;

connecting said memory array to said common node; and

placing an isolation circuit between each of said transmission lines and said common node.

8. The method of claim 8, further comprising:

providing control inputs to said isolation circuit to select one of said bus masters to drive a clock inputs to said memory array while isolating the transmission lines of the other bus masters from said common node.

9. A circuit comprising:

a plurality of transmission lines coupled between respective bus master clock outputs and a common node;

a plurality of memory modules coupled to said common node; and

an isolation circuit coupled between said plurality of transmission lines and said common node.

10. The circuit of claim 9, further comprising:

control means connected to said isolation circuit, said control means being configured to select one of said bus master clock outputs to drive to said memory modules, while selecting the transmission lines associated with the other bus master clock signals for isolation from said common node.

11. The circuit of claim 9, wherein a clock input of each of said memory modules is connected to said common node.

12. The circuit of claim 9, where said memory modules are SDRAM modules.

13. A method comprising:

connecting transmission lines from a plurality of memory bus masters to a common node;

connecting a memory array to said common node;

selecting one of said memory bus masters to drive clock outputs to said memory array; and

introducing a high impedance between the transmission lines of the other memory bus masters and said common node.

14. The method of claim 13, wherein said selected bus master is selected by control inputs from a memory bus arbiter.

15. The method of claim 13. wherein said high impedance comprises FETs.